PFC100W-12VPNE-PBF

(115Vac, 47- 800Hz Input)

100W, 12V/ 8.4A Single Output

Airborne PFC Power Module

Targeting low power avionics' applications, the **PFC100W-12VPNE-PBF** module provides an isolated 12Vdc output with an integral PFC input converter stage. It meets the most stringent airborne requirements including those for variable frequency 115Vac generator systems over the wide frequency range of 360-800Hz and RTCA/DO-160G category M emissions (with ext app note filter).

Utilizing thermal-clad circuit board technology and low profile planar magnetics, thermal gradients between heat dissipating components and the module baseplate are minimized while maintaining a low 0.75" profile. Accurate output regulation is assured by implementation of the module's remote sense feature. Standard protection features are built-in in to assure years of fault-tolerant and reliable operation in the harshest environments.

The **PFC100W-12VPNE-PBF** is capable of providing uninterrupted ride-through at full output load during momentary input AC brown-out conditions for up to 5mSec. Hold-up time is readily expanded by connecting external electrolytic capacitors to the PFC output pins provided.

Weighing less than 16 ounces, the **PFC100W-12VPNE-PBF** is housed in a silicon-based encapsulated enclosure with outer dimensions of 5.0" x 3.0" x 0.75". Four corner mounting holes are included to facilitate system mounting. The **PFC100W-12VPNE-PBF** is intended for low-profile PCB mount applications where the top-side baseplate can be flush mounted to LRU chassis sidewalls or a stand-alone heatsink.

The **PFC100W-12VPNE-PBF** is tuned to limit input power to **155W +/-6W** in order to control/ limit inrush current.

FEATURES

	Meets both RTCA/DO-160G, section 16, and Airbus ABD0100.1.8.1 issue C for power factor and input current harmonic distortion levels over the wide frequency operating range (360Hz – 800Hz) at ½ to full rated load
	Wide input range: 96Vrms – 134Vrms, 47 – 800Hz
	Complies with RTCA/DO-160G for conducted emissions, susceptibility and power input (section 16)
	Active inrush current limiting: < 4Apk typical, 7Apk maximum
	Size: 5.0" x 3.0" x 0.75", Weight: less than 16 ounces
	Tightly regulated isolated output: 12V / 8.4A
	Overcurrent protection with pulse-retry current limiting
	Two independent output overvoltage protection circuits. 13.3V "soft" with auto restart, 16V "hard" latching
	PFC output overvoltage protection with automatic restart (internal 200Vdc PFC output)
	Over-temperature shutdown with automatic restart (baseplate at or above 100°C)
	Under-temperature inhibit with set point program capability
	DC output valid status line (TTL)
	AC valid status line (TTL)
	Remote sense capability
	MTBF: 602,400 Hours (RIAC 217Plus, Aic, 50°C operating temperature, 65% DC, 2190 Cycles/ yr.)

Pb lead-free

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PPI POWER

PERFORMANCE SUMMARY

PARAMETER	SPECIFICATIONS
Voltage regulation	+12.2Vdc +/-2%
Rated output current	8.4A
Pk-Pk Ripple + Noise (20MHz)	180mVpp maximum
Module Efficiency	81% typical at full load
Output overcurrent threshold (1, 9)	9A typical
12V Soft overvoltage set-point (2)	13.3V +/- 3%
12V Hard overvoltage set-point (6)	16V +/- 3%
PFC output overvoltage set-point (2)	230V +/- 5%
Input to Output Isolation Voltage (8)	1500Vac minimum
Input to Chassis Isolation Voltage (3)	1500Vac minimum
Output ride-through / full load (4)	5mSec
Line to Line Input Capacitance (nom)	0.15uF
Minimum load (5)	n/a

Notes:

1. 9A typical (10.5A maximum) with pulse-retry current limiting and auto recovery into full load. Pulse is ~160mSec on and 2.3 seconds off in OCP mode.
2. Auto recovery
3. Primary to chassis, 1500Vac, 60Hz for 60 seconds without arc or damage; 3.0mArms maximum leakage current (line-to-earth capacitors installed)
4. 66uF internal hold-up capacitance, expandable by external capacitors. See application section for details.
5. No minimum load is required.
6. Latching fault, requires toggling input AC to reset. Full 8.4A output load
7. For some load conditions output may overshoot to 13.5Vpk at start up
8. Primary to secondary, 1500Vac, 60Hz for 60 seconds without arc or damage; 3.0mArms maximum leakage current (line-to-earth capacitors installed)
9. A fuse is required external to the module in the line lead as there is no overcurrent protection circuitry within input converter. See application circuit for details

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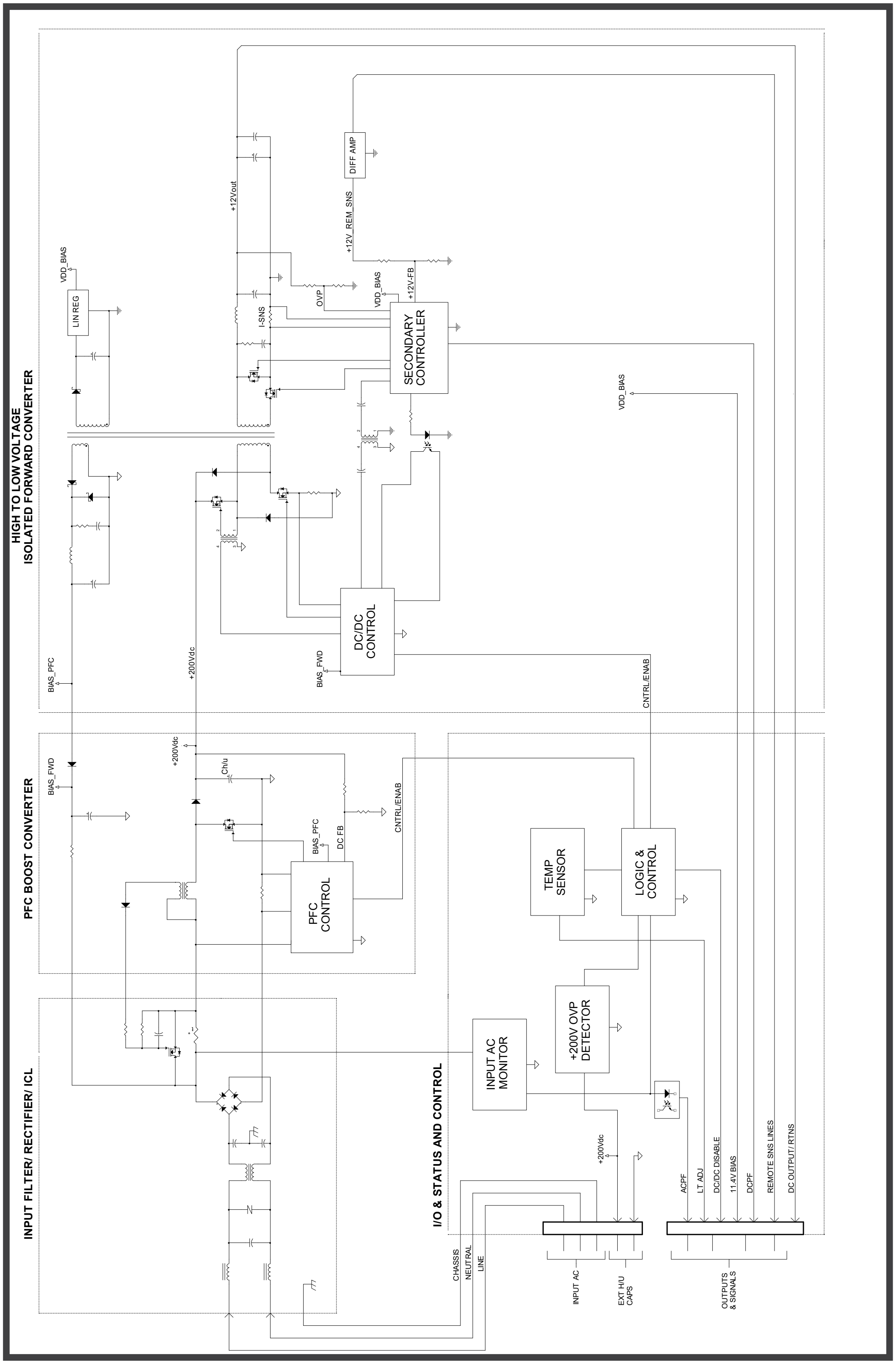
BLOCK DIAGRAM



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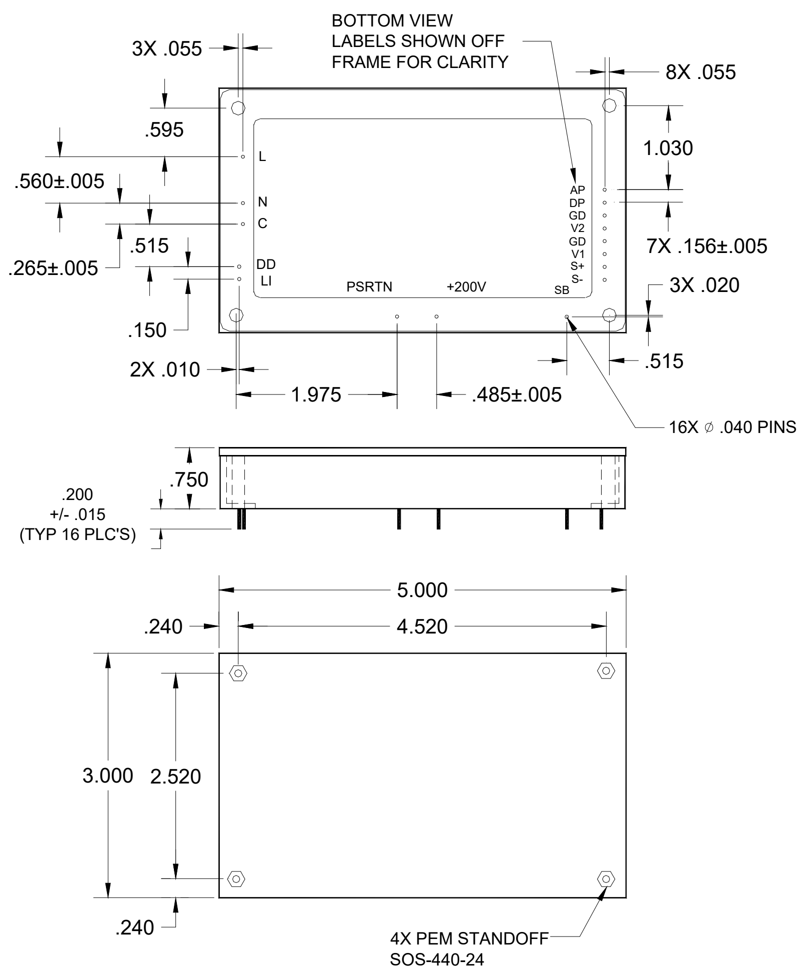
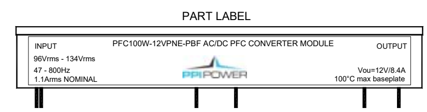
MECHANICAL DIAGRAM





PIN OUTS
L = Line
N = Neutral
C = Chassis
DD = DC/DC Disable
LI = Low Temp Inhibit
+200V = Pos terminal of ext Ch/u
PSRTN = Neg terminal of ext Ch/u
SB = Secondary Bias
AP = ACPF-L
DP = DCPF-L
GD = Output DC Return
V2 = 12V Output
GD = Output DC Return
V1 = 12V Output
S+ = Remote sense (+)
S- = Remote sense (-)

*** BASEPLATE FLATNESS**

Maximum warpage not to exceed

0.04” per 5” unit length.

A DETAILED OUTLINE DRAWING CAN BE FURNISHED UPON REQUEST

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ELECTRICAL SPECIFICATIONS

Unless otherwise specified the following parameters will be met over the specified operating temperature range of –40°C to +70°C, constant active load applied to the 12V output, 470uF Panasonic FR series electrolytic capacitor installed on 12V output terminals, Ch/u (external) = 1000uF, Vin = 115Vrms, 360Hz – 800Hz, <1.25% sinusoid. See notes following output characteristic table for details.

INPUT CHARACTERISTICS

PARAMETER	PFC100W-12VPNE-PBF	REMARKS	NOTES
INPUT VOLTAGE RANGE	96 – 134Vrms	Complies with power quality and normal / abnormal input voltages per DO-160G, sect. 16.	2
MUST START VOLTAGE	96Vrms minimum	Module will start and remain enabled for input voltage in the range of 96Vrms < Vin < 134Vrms.	2
MUST INHIBIT VOLTAGE	89Vrms maximum	Module output will inhibit following ~800mSec turn-off delay upon detection of input undervoltage <u><</u>89Vrms. 12V output to disable monotonically and remain disabled as long as input voltage remains <u><</u>89Vrms.	2
INPUT FREQUENCY RANGE	47 – 800Hz	Reduced distortion performance below 360Hz.	2
EFFICIENCY	80% minimum	Full output load (100W). 81% typical full load efficiency. See efficiency curve.	2
LEAKAGE CURRENT	< 2mArms	AC Line / Neutral to Chassis at 115Vrms / 400Hz.	1
INRUSH CURRENT	< 7Apk max, 9Apk max +25°C to +70°C	Cold or warm start; < 4Apk typical.	2
LINE TO NEUTRAL CAPACITANCE	150nF +/- 20%	X2 rated, 275Vac	1
LINE/ NEUTRAL CAPACITANCE TO CHASSIS GROUND	3000pF +/- 10%	X1,Y2 rated, 250Vac	2
Athd INPUT CURRENT	< 5.0%	50% - 100% output load (50W - 100W).	2
INDIVIDUAL HARMONICS AC CLEAN	EVEN: <1% If / n (n < 10) EVEN: <0.1%If (n <u>></u>10) ODD: <30% If / n ODD TRIPLENS:<15% If /n	If = Fundamental current Vthd < 1.25% n = order of harmonic (1 - 40) 50% - 100% output load (50W - 100W). Harmonics < 10mA disregarded. With or without app note filter.	1

PPI POWER

INPUT CHARACTERISTICS—CONTINUED

PARAMETER	PFC100W-12VPNE-PBF	REMARKS	NOTES
INDIVIDUAL HARMONICS DISTORTED INPUT	EVEN: <1% If / n + 1.25Vn (n < 10) EVEN: <0.1%If + 1.25Vn (n ≥ 10) ODD: <30% If / n + 1.25Vn ODD TRIPLENS:<15% If /n+1.25Vn	If = Fundamental current Vthd > 10% (clipped method), n = order of harmonic (1 - 40) Vn = corr input voltage harmonic. 50% - 100% output load (50W - 100W) +23° to +70°C 55% - 100% output load (55W - 100W) -40°C to +23°C Harmonics < 10mA disregarded. With or without app note filter.	1
QUIESCENT POWER	6.8W typical	No load applied to output.	1
POWER FACTOR	0.98 min	Pout > 50W at 360-440Hz Pout > 75W at 800Hz. With or without app note filter.	2
CREST FACTOR (CURRENT)	1.314 – 1.514	Ratio of peak / RMS.	1
START-UP TIME	< 750mSec, Tamb = +0°C to +70°C < 5 Seconds, Tamb = -40°C to -15°C < 2 Seconds, Tamb = -15°C to 0°C	Output within proper regulation.	2, 7, 10
CONDUCTED EMISSIONS	RTCA/DO-160G	Section 21, category M.	1, 4, 8
STORAGE TEMPERATURE RANGE	-55°C to +100°C	Non-operational.	1
OPERATING TEMPERATURE RANGE	-40°C to +70°C	Observe maximum baseplate temperature of +100°C.	1
LOW TEMPERATURE INHIBIT	0°C ± 3°C	Module's 12V output is inhibited at or below 0°C. Auto restart occurs when temperature rises above 0°C. The low temperature inhibit set point can be adjusted lower using one external low power resistor installed between LI pin and PSRTN pin, see application section for details.	1
OVERTEMPERATURE SHUTDOWN	100°C ± 5°C	Module's 12V output is inhibited at or above 100°C. Auto restart occurs at ~ 80°C baseplate temperature. Output may toggle at transition point due to pulse retry overcurrent protection circuit.	1
DC/DC CONV DISABLE-L	0.5V Maximum	Module's DC/DC converter can be disabled by applying a logic low to DD pin with respect to PSRTN pin. Delay time from application of logic low to converter disabling is <1mSec. Float DD pin to enable DC/DC converter.	1

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PPI POWER

OUTPUT CHARACTERISTICS

PARAMETER	PFC100W-12VPNE-PBF	REMARKS	NOTES
RATED OUTPUT POWER	100W	Observe maximum allowable baseplate temperature of 100C; see application information for details. Derate output power in accordance with allowable Pout versus ambient temperature curves.	2
OUTPUT VOLTAGE	12.2Vdc +/-2%	No load to full load (100W).	2, 7
OUTPUT OVERCURRENT THRESHOLD	9A typical, 10.5A maximum	Output current and voltage will foldback with pulse retry current limiting circuit. Pulse retry duty cycle is ~160mSec on and ~2.3 seconds off in OCP mode, cyclic mode as long as fault persists. No damage will occur to module during indefinite output short circuit conditions. Output will auto recovery into full rated load when fault clears.	2
TEMPERATURE STABILITY COEEFICIENT	0.05% / °C	Output voltage variation with temperature (500uV/°C).	1
OUTPUT RIPPLE + NOISE	180mVpp maximum	20MHz bandwidth. 100mVpp typical. Can be reduced with external capacitors, see application notes.	2
LINE REGULATION	<0.5%	Output deviation for +/- 20% step change in input voltage.	1
LOAD REGULATION	Output remains within 12.2V+/-5% regulation band.	50% step change in output load. Full load to half load or half load to full load. 10uSec rise/fall time. Output deviation can be reduced with inclusion of external bulk electrolytic capacitors (470uF or 1000uF).	1, 7
MINIMUM LOAD	0A	No minimum load is necessary for proper output regulation.	2
HOLD-UP TIME	5mSec nominal	No external hold-up capacitor attached. Requires external 250V rated capacitors to extend hold-up time. May be affected by warm start delay, see application section for details.	1
MAXIMUM EXTERNAL HOLD-UP CAPACITANCE	2800uF	Specified in order to not overstress the internal inrush current limiting circuit	1
ISOLATION VOLTAGE INPUT TO CHASSIS	1500Vac, 60Hz	No arcing or damage for 60-second test duration (3.0mArms max leakage). EMI caps installed.	2, 5, 8
ISOLATION VOLTAGE INPUT TO OUTPUT	1500Vac, 60Hz	No arcing or damage for 60-second test duration (3.0mArms max leakage). EMI caps installed.	2, 6, 8
INSULATION RESISTANCE OUTPUT TO CHASSIS	500Vdc	200M-ohms minimum	2, 8, 9
INSULATION RESISTANCE INPUT TO CHASSIS	500Vdc	200M-ohms minimum	1, 8, 9
INSULATION RESISTANCE INPUT TO OUTPUT	500Vdc	200M-ohms minimum	1, 8, 9

Pb lead-free

OUTPUT CHARACTERISTICS—CONTINUED

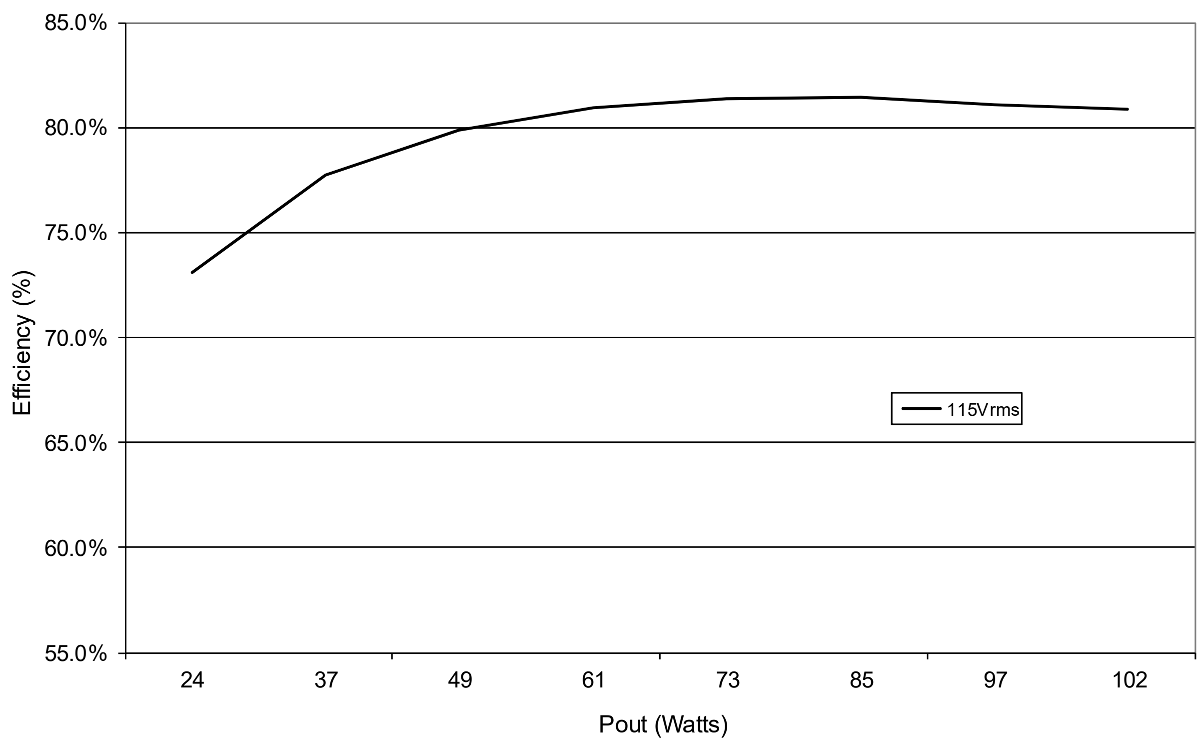
PARAMETER	PFC100W-12VPNE-PBF	REMARKS	NOTES
DCPWRFAIL-L (DP)	Transitions to TTL low (0.5Vmax) when 12Vdc output is detected outside of proper regulation window by >7.5%	TTL level, 3mA max sink current. Time to activation on a fault is 1mSec typical, 2.5mSec maximum.	2
ACPWRFAIL-L (AP)	Transitions to TTL low (0.5Vmax) upon detection of invalid input AC (≤ 89Vrms from 0% - 100% load)	TTL level, 16mA max sink current, 5mSec maximum delay time to activate on loss of input AC.	2
PFC 200Vdc OUTPUT	200Vdc ± 3%	10W ≤ Pout < 100W.	2, 3
MINIMUM DC/DC CONVERTER OPERATING VOLTAGE	95Vdc	Minimum amplitude for PFC output that will guarantee proper output regulation for the 12V output.	1
OUTPUT OVERVOLTAGE PROTECTION "SOFT"	13.3V ± 3%	Pulse by pulse protection (inner loop), auto-restart.	1
OUTPUT OVERVOLTAGE PROTECTION "HARD"	16V ± 3%	Module will be latched off if output is detected at or above this level. 12V output may rise higher than detection point until latch off process is complete. Requires recycling of input AC to reset module. Full 8.4Aload.	1
OUTPUT OVERVOLTAGE PROTECTION (PFC 200Vdc OUTPUT)	230V ± 5%	PFC output is clamped to this level if control loop regulation is lost, auto-recovery.	1
SB OUTPUT	9.4V +/- 10%	Secondary referenced low current bias voltage available for general purpose use. This pin is labeled SB and can provide up to 25mA and is internally protected against output short circuit conditions. SB is only available when DC/DC converter is enabled (no fault condition) and 12V output is present.	1

Notes:

1. Ensured by design, not 100% tested in production.
2. 100% tested for specification compliance at 23°C ambient in production.
3. 200Vdc PFC output voltage tolerance is +/-5% for Pout < 10W.
4. Requires external differential / common-mode filter installed on power lines for full compliance, see application section for details.
5. When performing input to chassis isolation voltage testing at the module level it is recommended to tie the primary referenced terminals: Line, Neutral, LI, DD, +200V and PSRTN together and hi-pot all of these with respect to chassis ground.
6. When performing input to output isolation voltage testing at the module level it is recommended to tie the primary referenced terminals: Line, Neutral, LI, DD, +200V and PSRTN together and hi-pot all of these with respect to all of the secondary referenced terminals which are also tied together (this includes AP, DP, GD, VO, SB, S+ and S-).
7. For some load conditions output may overshoot to 13.5Vpk at start up .
8. Not verified over full operating temperature range of –40°C to +70°C.
9. After 5-sec minimum or until IR value has steadied; this may take upwards of 60-secs depending on safety tester and voltage ramp rates.
10. Output may take several seconds to start at low line voltage with high values of hold-up capacitance and /or increase in resistance of inrush-current limiting thermistor at cold temperature.

EFFICIENCY CURVE

Efficiency data at nominal input: Vin = 115Vrms, 400Hz and room temperature (23°C)



TEMPERATURE CHARACTERISTICS

*AIRFLOW (LFM)	THERMAL IMPEDANCE (Θ_{s-a}) (no external heatsink)
0 LFM	3.4 °C/W
250 LFM	1.0 °C/W
500 LFM	0.6 °C/W

* Air velocity measured using a digital anemometer positioned within an airflow duct 3" X 3" above top of module

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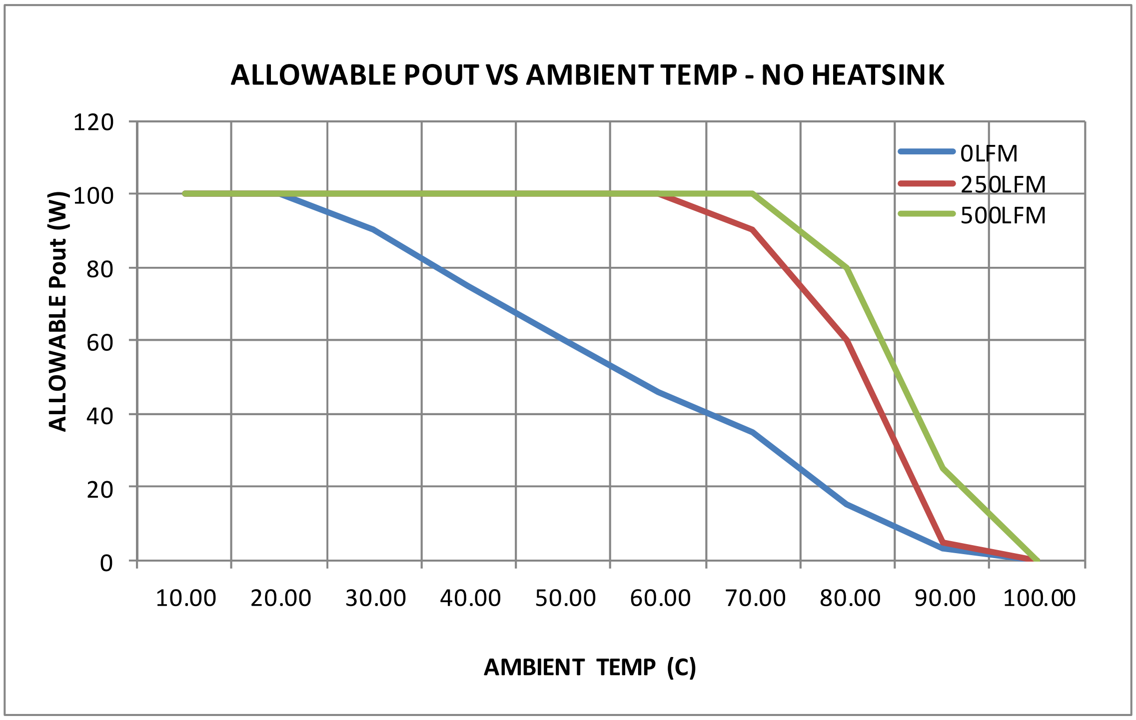
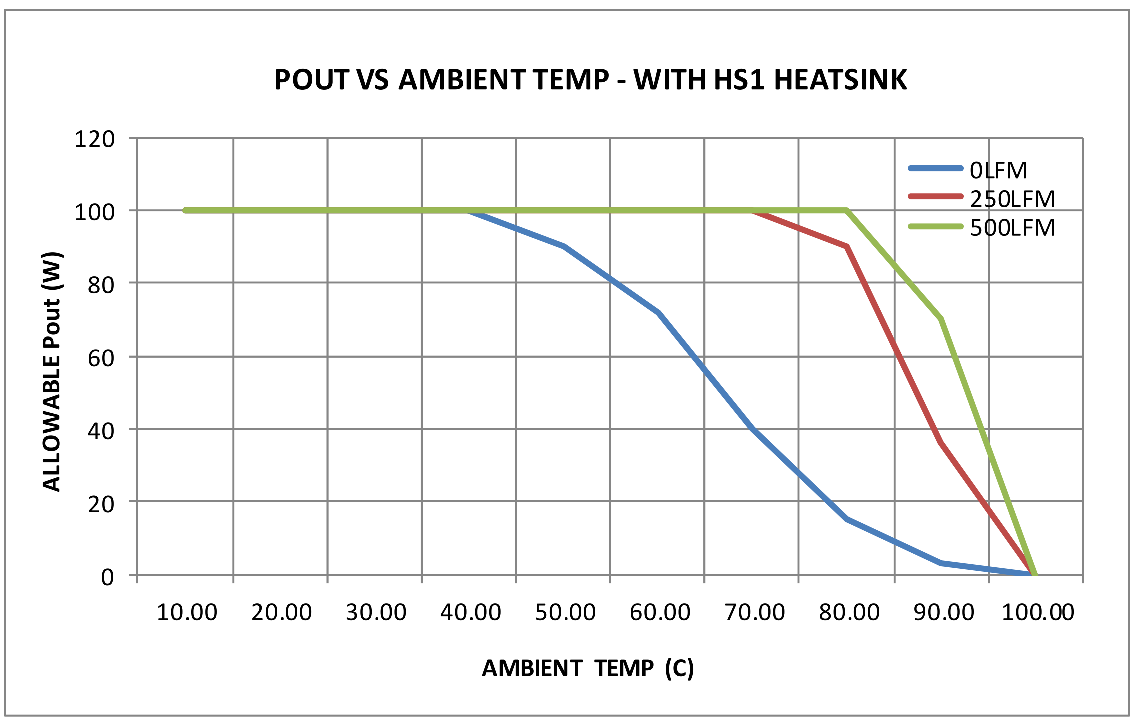
POWER DERATE CURVES





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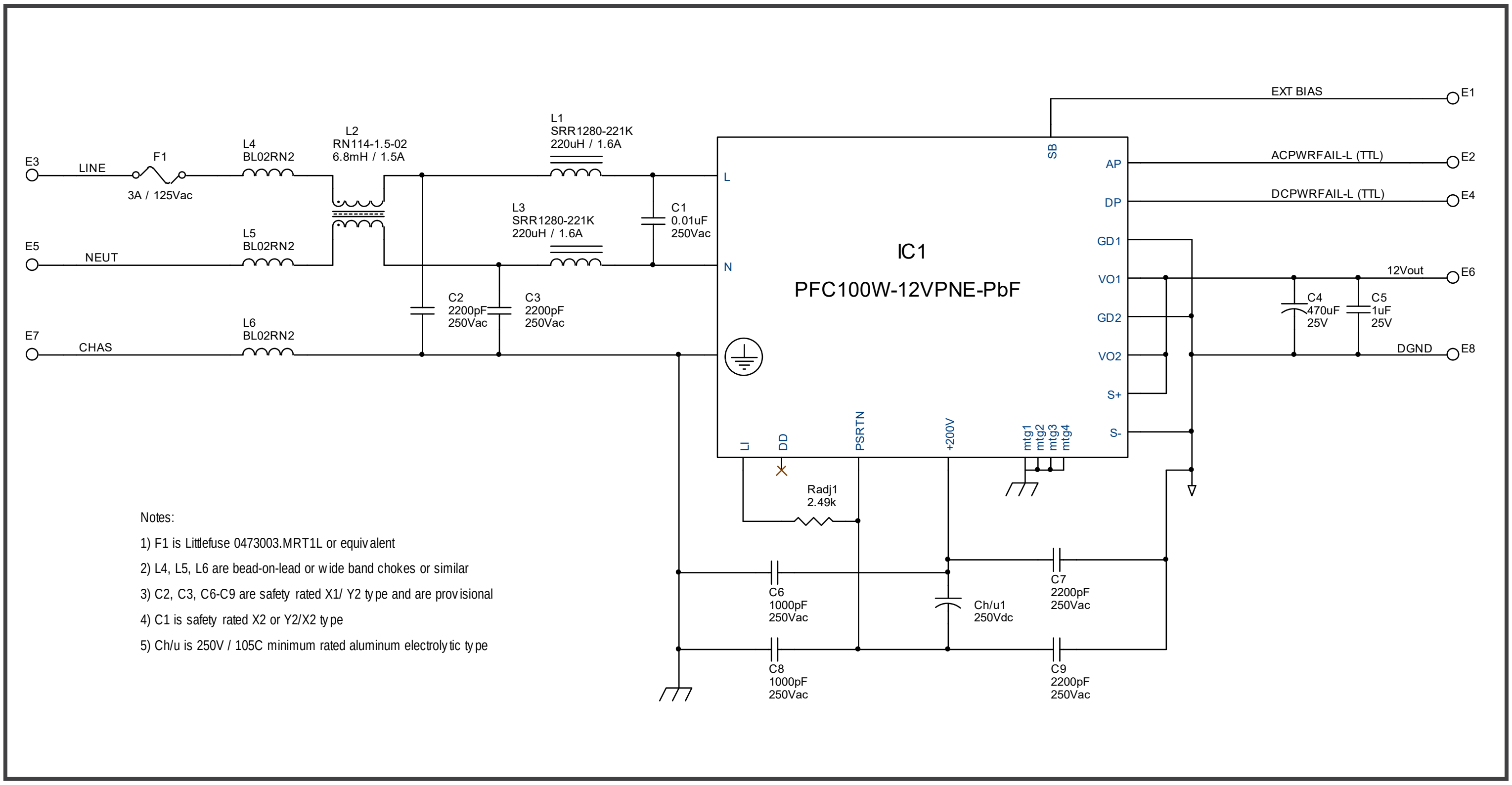
APPLICATIONS INFORMATION



Typical Application Circuit

Caution:

Hazardous live voltages present on module terminals. Take precautions when operating circuit to avoid injury.

A 3A/ 125Vac external fuse is required in the line lead as shown in the application circuit as the module does not contain input overcurrent protection circuitry

HOLD-UP TIME

The PFC100W-12VPNE-PBF module provides two interconnecting pins in order to extend hold-up time with external capacitors. In order to extend module hold-up time, polarized 250V (minimum) electrolytic capacitors must be connected externally between the module's +200Vpin and PSRTN pin. Required external capacitance can be determined using the following formula:

$E = P * (t + t_{restart}) = (0.9) * \{½\ C_{h/u\ (total)}\ (Vi^2 - Vf^2)\}$

Where,
P = output power (Watts)
t = desired hold-up time (Seconds)
$t_{restart}$ = warm start delay of approximately 20mSec upon reapplication of input AC
$C_{h/u\ (total)}$ = total hold-up capacitance (Farads), includes internal 53uF (minimum) and external capacitance
$C_{h/u\ (ext)}$ = external hold-up capacitance (Farads)
0.9 factor constitutes internal DC/DC converter efficiency
Vi = Minimum PFC voltage of 194Vdc (200Vdc - 3%)
Vf = 100Vdc

$E = P * (t + t_{restart}) = (0.9) * \{½\ C_{h/u}\ (Vi^2 - Vf^2)\}$

In order to hold up 100W output power for 200mSec requires:

$C_{h/u\ (total)} = \{(100W)\ (200mSec + 20mSec)\} \div \{(1/2)\ (0.9)\ (194V^2 - 100V^2)\} = 1770uF$

$C_{h/u\ (ext)} = C_{h/u\ (total)} - 53uF = 1770uF - 53uF = 1720uF$ (minimum)

Use of 105°C, 250Vdc, 20% tolerance snap-mount aluminum electrolytic capacitors is recommended. For the example above, a total nominal capacitance of 2150uF would be necessary to assure the required capacitance of 1720uF was achieved. Warm start delay occurs for AC power interrupts greater than 25mSec as a result of combination of time to reactivate PFC control circuitry, reinitiation of PFC soft-start cycle and reaching module power limit.

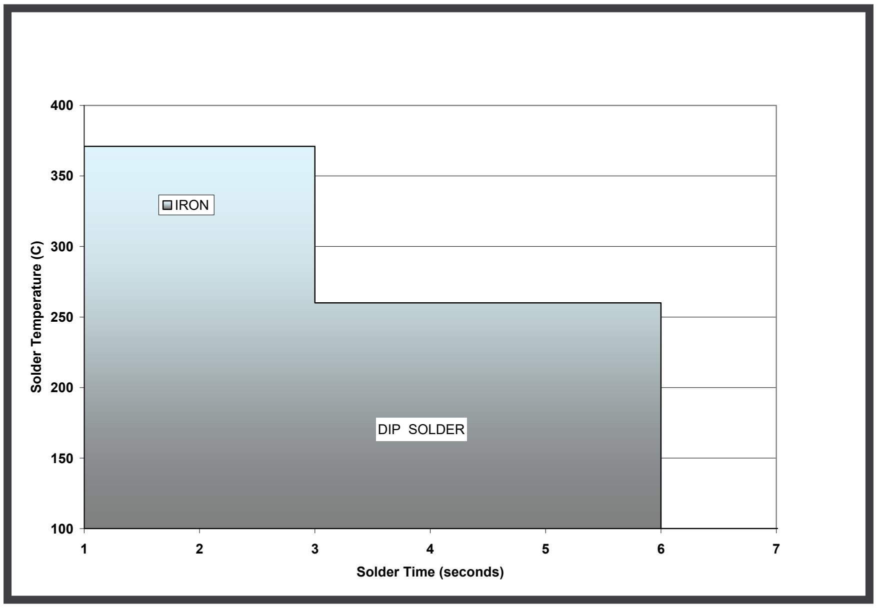
PLACEMENT, FLATNESS AND MOUNTING

The PFC100W-12VPNE-PBF module may be flush mounted and soldered to a PCB. The baseplate (topside) may be mounted to a flat surface for heatsinking or to a stand-alone heatsink. If mounting the baseplate to a flat surface a thermal interface pad is recommended as some warpage of the module's aluminum baseplate may exist. Warpage of the baseplate surface (including bow and twist) occurs in the manufacturing of the internal thermal clad circuit board and is a result of high temperatures required during the lamination process as well as during the panel cutting process. Baseplate warpage is limited to 0.04" per 5" unit length. Temperature activated thermally conductive interface pads, such as Chomeric's T725 series, are suitable interface pads for this application.

The PFC100W-12VPNE-PBF module contains 4 corner threaded #4 mounting holes (see mechanical diagram for details). The standard mounting hole configuration is partially threaded; threaded approximately 0.44" through from the baseplate side of the module.

SOLDERING INFORMATION

In order to minimize mechanical force exerted on the module pins, the module should be mechanically fastened to the printed circuit board prior to soldering each of the I/O pins. The pins are soldered internally to the module's horizontal through-hole circuit board using a high temperature solder that allows for application of high heat for long time durations when soldering the module to an external circuit board without concern for re-flow of the internal solder joints. The allowable heat application versus time duration curve is shown below and should be adhered to in order to prevent re-flow of the module pins internal solder joints.



ROUTING CONSIDERATIONS

Assure there is at least 4.2mm between primary referenced and secondary referenced signals. Secondary referenced signals include AP, DP, V1, V2, GD, SB, S+ and S-. Avoid routing secondary referenced signals directly beneath module on component layer.

REMOTE SENSE LINES

Remote sense capability is provided in order to "margin-up" the 12V output to overcome small system level voltage drops in traces and connectors. If using the remote sense lines, the maximum allowable system level voltage drop (or combined differential voltage between Vout and +SNS and DGND and –SNS) is 700mV. Exceeding this amplitude may force the module's overvoltage protection circuit to activate. If not using the remote sense line feature at a remote point-of-load, each sense line should be terminated at the output pins of the module (+SNS to Vout and –SNS to DGND). Remote sense lines should be connected directly to the +12V and DGND power forms prior to any additional inductive filter elements that may be included.

CAPACITIVE LOADING AND PROPER POWER-UP CONSIDERATIONS

Avoid applying full (8.4A) load current to the module's output prior to allowing the output to reach at least 6Vdc to avoid module latch-up when starting. Module latch-up can occur under certain power-up modes (e.g., low line) if the module enters internal power-limit prior to its internal bias voltages reaching minimum operating levels. If implementing active loading on the modules output (constant current sink), assure that the turn-on voltage of the active load instrument is set to at least 6Vdc. If implementing external bulk capacitors on the module's 12V output, assure proper power-up under all input line and output load conditions.

EMI CONSIDERATIONS

Use of a chassis ground plane beneath module on first internal circuit board layer (beneath component layer) of PCB is recommended. Assure that sufficient isolation distance exists between chassis plane and each of the modules input and output pins such that there is at least 4.2mm between primary referenced and secondary referenced signals. Although the PFC100W series modules contain internal common-mode and differential mode input filtering the use of a small external inductive based line filter is recommended for EMI compliance. See application circuit for suggested filter arrangement. Reduce or eliminate line-to-line capacitance (C1) for applications operating at low power levels (<60W output) as it may have an adverse effect on input current harmonic distortion at higher line frequencies (e.g., 800Hz).

If external hold-up capacitors are more than 3 inches away from module, 1000pF decoupling capacitors (line-to-earth rated) should be installed between +200V signal & chassis ground and PSRTN signal & chassis ground in close proximity to respective module terminals.

In order to reduce differential peak-to-peak ripple + noise on the 12V output voltage, adding a parallel combination of low ESR electrolytic and MLCC ceramic capacitors from V1/V2 to GD is recommended. Recommended low ESR electrolytic capacitors include Panasonic FC or FR series for the 12V output and AVX Flexiterm for the MLCC capacitors. In order to assure output voltage stays within proper regulation during 50-100% transient load testing or conditions at cold temperatures (<0°C) additional low ESR electrolytic capacitors attached to the output terminals of the module may be required (e.g., parallel 470uF or single 1000uF, 25V caps).

LOW TEMPERATURE INHIBIT CIRCUIT

The module contains a thermal sense circuit dedicated to inhibit the module if the ambient temperature is sensed below 0°C +/- 3°C. When the ambient temperature is sensed lower than 0°C the modules internal DC/DC converter is disabled removing the 12V output (the PFC converter remains enabled during this time). The DC/DC converter will start automatically if the ambient temperature is sensed higher than 0°C +/- 3°C. This set point can be adjusted lower by inclusion of an external low power rated programming resistor installed between the LI pin and PSRTN pin. The adjustment resistor (Radj) value versus temperature inhibit set point is tabulated below.

Inhibit Set Point (°C)	Radj (ohms)
-40	1.18k
-35	2.00k
-30	3.16k
-25	4.64k
-20	6.98k
-15	11.0k
-10	18.7k
-8	24.9k
-5	42.2k
0	DNP

Pb lead-free

THERMAL CONSIDERATIONS

There is no derating required for module output power up to the module baseplate temperature of 100°C. Beyond this temperature the module will shutdown. Allowable output power draw must be derated for elevated ambient temperatures if module baseplate temperature is not controlled or maintained below 100°C maximum. Refer to thermal derating curves for allowable power levels versus ambient temperature. The curves provide for allowable Pout versus ambient temperature for module with or without HS1 heatsink with 0LFM, 250LFM and 500LFM forced air cooling. HS1 heatsink can be purchased separately for this module. Contact PPI for further information.

In order to assure the baseplate temperature remains below 100°C additional heatsinking or forced airflow may be required. In order to estimate baseplate temperature and whether external heatsinking or airflow is necessary, apply the following formulas:

$T_{baseplate} = T_{ambient} + (P_{diss})(\Theta_{s\text{-}a})$

Where:
$T_{baseplate}$ = module baseplate temperature in °C,
$T_{ambient}$ = ambient air temperature in °C,
$\Theta_{s\text{-}a}$ = thermal resistance from module baseplate to ambient air in °C/W without external heatsink,
eff = efficiency from curve,
$P_{diss} = \{(P_{out} \div \text{eff}) - P_{out}\}$ in watts

As an example,
Assume a desired output power of 75W at nominal line operation (115Vrms) with a maximum ambient temperature of 70°C. The following formula would apply:

$T_{baseplate}$ = 70°C + {(75W / 0.81) – 75W)} (3.4°C/W) = 130°C

Therefore either an external heatsink would be required or forced airflow such that $\Theta_{s\text{-}a}$ was reduced to:

$\Theta_{s\text{-}a} < \{(T_{baseplate} - T_{ambient}) \div P_{diss}\}$